REMARKS

The comments of the Applicant below are each preceded by related comments of the Examiner (in small, bold type). The page and line numbers below refer to those in the application as originally filed, and the paragraph numbers refer to those of the published application.

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "each pixel consists of two ratioed sub pixels" (claim 21) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

FIG. 7 of Applicant's specification shows a plurality of pixels in which each pixel consists of two ratioed sub pixels. For example, a first pixel has sub pixels X+1 and X+2, a second pixel has sub pixels X+3 and X+4, a third pixel has sub pixels X+5 and X+6, a fourth pixel has sub pixels X+7 and X+8. See page 9, lines 16-19.

35 U.S.C. 112

Claims 1-8 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Regarding claim 1, "wherein the device is operable in a first mode in which the plurality of sub-pixels of a pixel are addressed simultaneously with a data signal and in a second mode in which the sub pixels of a pixel are addressed individually with respective data signals" is not described in such a way that enables one skill in the art to understand how two different modes of display be in one display device. In those two different modes of display, the TFT's are connected in two different ways. How those two different circuit arrangements fit in one display device?

In the two modes of operation recited in claim 1, the TFTs are not connected in two different ways. Rather, the TFTs are switched differently. The two modes of operation refer to different ways of driving the voltages on the column and row conductors to address the sub pixels.

FIG. 2 of Applicant's specification shows an example of a pixel that can operate in two modes. Operation of the pixel of FIG. 2 in the first mode is described in page 7, lines 17 to 25,

and operation of the pixel of FIG. 2 in the second mode is described in page 6, line 19 to page 7, line 6.

FIG. 3 of Applicant's specification shows another example of a pixel that can operate in two modes. Operation of the pixel of FIG. 3 in the first mode is described in page 7, lines 17 to 25, and operation of the pixel of FIG. 3 in the second mode is described in page 7, lines 7 to 16.

Also see paragraphs [0009], [0013], [0030], and [0031], and the Abstract of Applicant's specification for support of claim 1.

Claims 1-18, 21, 22-26, 28, 29-32 and 33-35 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 1 and 13

Applicant's specification describes row and column drive circuits that are "selectively controllable by the timing and control unit 45" in response to a mode selection control signal MS applied thereto so as to switch the manner of operation of these circuits between that required for a low power mode of operation of the pixels and that required for a video mode of operation of the pixels" (page 8, lines 29-32).

Claim 15

For the pixel shown in FIG. 2 of Applicant's specification, when operating in the first mode (which corresponds to the video mode), the switches T2 to T4 of all pixels in the array can be held on for the duration of this operational mode (page 7, lines 17-27). When operating in the second mode (which corresponds to the low power mode), the switches T2 to T4 are only turned on for a portion of the time, as shown by the timing diagram of FIG. 4 (labeled "Row n+1," "Row n+2," and "Row n+3") (page 6, line 21 to page 7, line 2). Therefore, the switches T2 to T4 are turned on during the first mode of operation for a period of time longer than that during the second mode of operation.

For the pixel of FIG. 3 of Applicant's specification, when operating in the first mode (which corresponds to the video mode), the switches T2 to T4 of all pixels in the array can be held on for the duration of this operational mode (page 7, lines 17-27). When operating in the second mode (which corresponds to the low power mode), the switches T2 to T4 are only turned on for a portion of the time, as shown by the timing diagram of FIG. 5 (labeled "Row n+1," "Row n+2," and "Row n+3") (page 7, lines 8-9). Therefore, the switches T2 to T4 are turned on during the first mode of operation for a period of time longer than that during the second mode of operation.

Claim 17

Applicant's specification describes that by appropriate control of the switches (T1-T4) the pixels can be driven in a first mode in which the common switch (T1) is operated to control the simultaneous addressing of the sub pixels (P1-P4) with a data signal, for example, for a video display with full grey scale capability, and in a second mode in which the switches (T1-T4) are controlled sequentially to allow different data signals to be applied to the individual sub pixels, for example, as required for a low power standby mode of operation with limited grey scale and color capability. See page 12, line 29 to page 13, line 4, and page 3, lines 9 to 12.

Claim 18

Applicant's specification describes a method of operating a display in a low power mode in which sub pixels of the display device are driven to one of two states, a light state and a dark state (page 2, lines 1 to 3 and line 11). The light state and dark state correspond to the two levels that can be selected for the data signal of claim 18.

Claim 21

FIG. 7 of Applicant's specification shows a plurality of pixels in which each pixel consists of two ratioed sub pixels (page 9, lines 16-19).

Claim 22

FIG. 2 shows an example of a first switching transistor T1 and a second switching transistor T2.

FIG. 3 shows another example of a first switching transistor T1 and a second switching transistor T2.

Claim 25

Applicant's specification describes that a pixel may consist of two sub pixels one having an area A and a second having an area 2A (page 2, lines 9-10).

Claim 28

Applicant's specification describes that "the row and column drive circuits are selectively controllable by the timing and control unit 45 in response to a mode selection control signal MS applied thereto so as to switch the manner of operation of these circuits between that required for a low power mode of operation of the pixels and that required for a video mode of operation of the pixels" (page 8, lines 29-32).

Claim 29

Claim 29 has been amended.

Claim 31

Applicant's specification describes a display device that has red, green, and blue pixels (page 1, line 32 to page 2, line 1). Each of the red, green, and blue pixels corresponds to one color component of a pixel of claim 31.

Claims 32 and 33

Claims 32 and 33 have been amended.

35 U.S.C. 102

Claims 1-7, 9-12, 14, 19, 20, 22, 23, 26, 27, 29, 30, 32 and 33 are rejected under 35 U.S.C. 102(e) as being anticipated by Edwards et al. (US 7,230,597).

As to claim 1, Edwards et al. discloses an active matrix display device comprising

An array of pixels a set of row conductors through which rows of pixels are selected (fig. 1, col. 4, lines 64-67),

A set of column conductors through which data signals are supplied to selected pixels (fig. 1, col. 4, line 64- col. 5, line 13),

Each pixel comprising a plurality of sub pixels which sub pixels are each associated with a respective switching transistor for controlling the supply of a data signal to the sub pixel (figs. 1, 8, 9, col. 4, line 64 – col. 5, line 13),

Wherein the plurality of sub pixels of a pixel are coupled to a column conductor associated with the pixel via a common switching transistor through which data signals are supplied to the sub pixels (fig. 1), and

Wherein the device is operable in a first mode in which the plurality of sub-pixels of a pixel are addressed simultaneously with a data signal (fig. 9, col. 8, lines 44-48) and in a second mode in which the sub pixels of a pixel are addressed individually with respective data signals (fig. 8, col. 8, lines 35-40) (as best understood).

Claim 1

Applicant disagrees. Edwards does not describe and would not have made obvious "wherein the device is selectively operable in a first mode in which the plurality of sub-pixels of a pixel are addressed simultaneously with a data signal and in a second mode in which the sub pixels of a pixel are addressed individually with respective data signals," as recited in claim 1.

Edwards discloses two different drive schemes that are implemented using two different circuits. Edwards does not disclose or suggest a device that is selectively operable in two different modes, as recited in claim 1.

In FIG. 8 and column 8, lines 35-39, Edwards discloses a drive scheme in which plural address lines 14 are provided for each row separately controlling a plurality of thin film transistors 12 of a pixel, and the address lines 14 are individually selected to deliver each successive bit to the pixel sequentially. Edwards does not describe or suggest that a display device using drive scheme of FIG. 8 is selectively operable in two different modes.

In FIG. 9 and column 8, lines 50-59, Edwards discloses a way to transfer data to each of the capacitance 90 – 93. Initially the first, second, third and fourth address lines 80, 81, 82, 83 are all selected and data is supplied along column line 16 to be written to fourth capacitance 93. Then, the fourth address line 83 is deselected and a further bit of data applied to column line 16

to be written to third capacitance 92. After deselecting the third address line 82, the second capacitance 91 can be written. Finally, the second address line 81 can be deselected, leaving only the first address line 80 selected and data is written to the first capacitance 90. In the arrangement shown in FIG. 9 of Edwards, when the data is written to the fourth capacitance 93, the data is also written to the first to third capacitances. However, this is merely part of the process of transferring data to each of the capacitances 90-93. Edwards does not describe or suggest that a display device using the arrangement of FIG. 9 is "selectively operable" in two modes, the first mode being such that the plurality of sub-pixels are addressed simultaneously with a data signal and the second mode being such that the sub pixels of a pixel are addressed individually with respective data signals.

Claim 27 is patentable for at least similar reasons as those applied to claim 1.

As to claim 14, Edwards et al. discloses a display device comprising a timing and control unit, a row drive circuit, and a column drive circuit that are operable in the first mode to switch the switching transistors associated with the sub pixels of a pixel at the same time so as to supply a data signal on the associated column conductor to each sub pixel (fig. 9), and

Wherein the timing and control unit, row drive circuit, and column drive circuit are operable in the second mode to switch the switching transistors associated with the sub pixels of the pixel selectively in sequence such that data signals on the associated column conductor are supplied to respective sub pixels (fig. 8).

Claim 14

Edwards discloses two different drive schemes that are implemented using two different circuits. Edwards does not disclose or suggest a timing and control unit, a row drive circuit, and a column drive circuit that are operable in a first mode and a second mode, as recited in claim 14.

As to claim 19, Edwards et al. teaches an active matrix device comprising:

A plurality of pixels, each pixel having at least two sub pixels (figs. 1, 8, 9);

A plurality of column conductors and a plurality of row conductors for addressing the pixels (figs. 1, 8, 9, col. 4, lines 64-col. 5, line 13);

A first row conductor that controls a signal path between one of the pixels and one of the column conductors, the first row conductor controlling a signal path between two sub pixels of another pixel (figs. 8, 9); and

A second row conductor that controls a signal path between the other pixel and one of the column conductors (figs. 8, 9).

Claim 19

The Edwards '597 patent does not describe and would not have made obvious "a first row conductor that controls a signal path between one of the pixels and one of the column conductors, the first row conductor controlling a signal path between two sub pixels of another pixel," as recited in claim 19.

In each of FIGS. 8 and 9 of the Edwards '597 patent, the four capacitors 72 belong to a single pixel (see col. 8, line 24-26, which describes the capacitors 72 in FIG. 7 that are similar to those in FIGS. 8 and 9). FIGS. 8 and 9 of the Edwards '597 patent does not show a row conduct that controls "a signal path between one of the pixels and one of the column conductors" and "a signal path between two sub pixels of another pixel," as recited in claim 19.

As to claim 22, Edwards et al. discloses an apparatus comprising:
An array of pixels in which each pixel comprises at least one pair of sub pixels (figs. 1, 8, 9);
Column conductors each being connected to the pixels of one column of the array of pixels (figs. 1, 8, 9); and
Row conductors in which two or more of the row conductors are connected to the pixels of one row of the array of pixels (figs. 1, 8, 9), the circuit comprising:
A first switching transistor with its input terminal connected to the column conductor, its output connected to the first sub pixel in the pair, and its control terminal connected to the first row conductor (fig. 9); and
A second switching transistor associated with its input terminal connected to the output terminal of the first switching transistor, its output terminal connected to the second sub pixel in the pair, and its control terminal connected to the second row conductor. (fig. 9) (as best understood).
As to claim 26, Edwards et al. teaches an apparatus wherein at least some row conductors are connected to two pixels in the same column (fig. 8).

Claim 22

The Edwards '597 patent does not describe and would not have made obvious "row conductors each being connected to two pixels in the same column," as recited in amended claim 22.

In FIG. 8 of the Edwards '597 patent, each row conductor 80, 81, 82, and 83 is connected to one pixel in the same column. None of the row conductors 80, 81, 82, and 83 is connected to two pixels in the same column.

Claims 13, 15-18, 21, 28, 31, 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edwards et al. (US 7,230,597).

As to claim 13, Edwards et al. teaches a display device wherein the device is operable in a first mode in which the plurality of sub-pixels of a pixel are addressed simultaneously with a data signal (fig. 9, col. 8, lines 44-48) and in a second mode in which the sub pixels of a pixel are addressed individually with respective data signals (fig. 8, col. 8, lines 35-40).

Edwards et al. does not explicitly teach selectively switching between the first mode of operation and the second mode of operation I response to a mode selection control signal.

However, it is obvious that the display device of Edwards et al. is capable of selectively switching between the first mode of operation and the second mode of operation in response to a mode selection control signal in order to reduce power consumption (as best understood).

Claim 13

Edwards discloses two different drive schemes that are implemented using two different circuits. Edwards does not disclose or suggest a device that is selectively operable in two different modes, and does not disclose or suggest a timing and control unit that selectively switches between a first mode of operation and a second mode of operation in response to a mode selection control signal, as recited in claim 13.

All of the dependent claims are patentable for at least the reasons for which the claims on which they depend are patentable.

Canceled claims have been canceled without prejudice or disclaimer.

Any circumstance in which the applicant has addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner. Any circumstance in which the applicant has made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims. Any circumstance in which the applicant has amended or canceled a claim does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

No fee is believed to be due. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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